AMENDMENTS TO THE SPECIFICATION

Please delete the current Title, and replace it with the following new Title:

Semiconductor Integrated Circuit Device with Dual Insulation System

Please delete paragraph [0028], and replace it with the following new paragraph:

[0028] Referring again to FIG. 3, in operation, when an input signal IN1 is at a low level of ground voltage VSS and at least one of input signals IN2-IN5 is at a low level of a ground voltage VSS, internal node ND1 may be precharged to high voltage VPP through PMOS transistor MP2. In this case, the output signal OUT becomes a low level of the ground voltage VSS, so that PMOS transistor MP3 is also turned on. Since the gate of NMOS transistor MN4 (coupled to an internal power supply voltage IVC or an external power supply voltage EVC) is always in a turn-on state, a voltage of IVC-Vtnl is applied to the drain of NMOS transistor MN4 through NMOS transistor MN3. That is, a voltage applied to the drain of the NMOS transistor MN4 is restricted by NMOS transistor MN3 of the interface circuit 26. Accordingly, although NMOS transistor MN4 has a relatively thin gate insulation layer, the gate insulation layer of the NMOS transistor MN4 is not broken by the high voltage VPP, and a turn-on speed of NMOS transistor NM4 does not need to be lowered. Similarly, since IVC/EVC is always applied to the gate of the NMOS transistor MN3, a gate-drain voltage difference of NMOS transistor MN3 is VPP-IVC/EVC. Although NMOS transistor MN3 has a relatively thin gate insulation layer, the gate insulation layer of the NMOS transistor MN3 is not broken by the high voltage VPP.